ESP32-PICO-V3-02

Datasheet

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Espressif Systems

About This Document

This document provides the specifications for ESP32-PICO-V3-02.

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1 Overview

1.1 Features

MCU

- ESP32 embedded, Xtensa® dual-core 32-bit LX6 microprocessor, up to 240 MHz
- 448 KB ROM for booting and core functions
- 520 KB SRAM for data and instructions
- 16 KB SRAM in RTC

Wi-Fi

- 802.11 b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Bluetooth®

- Bluetooth V4.2 BR/EDR and Bluetooth LE specification
- Class-1, class-2 and class-3 transmitter
- AFH
- CVSD and SBC

Hardware

- Interfaces: ADC, DAC, touch sensor, SD/SDIO/MMC Host Controller, SPI, SDIO/SPI Slave Controller, EMAC, motor PWM, LED PWM, UART, I^2C, I^2S, infrared remote controller, GPIO, pulse counter, Two-Wire Automotive Interface (TWAI®, compatible with ISO11898-1)
- 40 MHz crystal oscillator
- 8 MB SPI flash
- 2 MB SPI PSRAM
- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating temperature range: –40 ~ 85 °C
- Dimensions: (7 × 7 × 1.11) mm

1.2 Description

The ESP32-PICO-V3-02 is a System-in-Package (SiP) device that is based on ESP32 with ECO V3 wafer, providing complete Wi-Fi and Bluetooth® functionalities. It integrates a 8 MB SPI flash and a 2 MB SPI PSRAM.

At the core of ESP32-PICO-V3-02 is the ESP32 (ECO V3) chip, which is a single 2.4 GHz Wi-Fi and Bluetooth combo chip designed with TSMC's 40 nm low-power technology. ESP32-PICO-V3-02 integrates all peripheral components seamlessly, including a crystal oscillator, flash, PSRAM, filter capacitors and RF matching links in one single package. Its assembly and testing are already done at SiP level. As such, ESP32-PICO-V3-02 reduces the complexity of supply chain and improves control efficiency.

With its ultra-small size, robust performance and low-energy consumption, ESP32-PICO-V3-02 is well suited for any space-limited or battery-operated applications, such as wearable electronics, medical equipment, sensors and other IoT products.

Comparing to other ESP32 series chips, ESP32-PICO-V3-02 has an additional pin GPIO20. For chip security purpose, flash pins DI, DO, /HOLD, /WP and PSRAM pins SI/SIO0, SO/SIO1, SIO2, SIO3 are not led out.

Note:

- For details on ESP32, please refer to the document *ESP32 Datasheet*.
- For details on ESP32 ECO V3, please refer to *ESP32 ECO V3 User Guide*.

1.3 Applications

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Building
- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications

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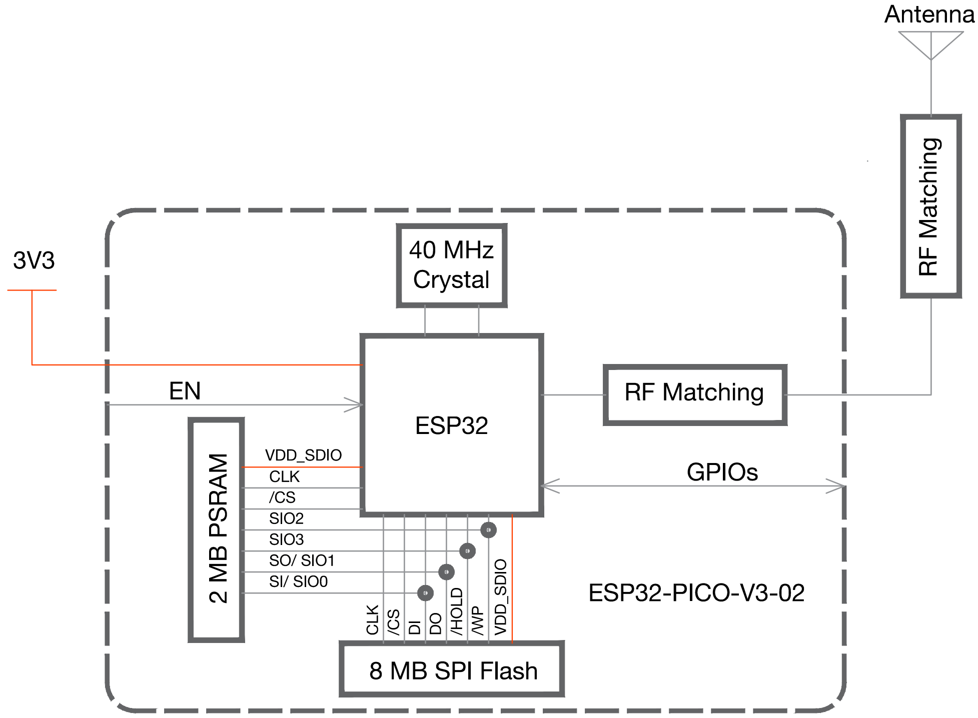


Figure 1: ESP32-PICO-V3-02 Block Diagram

3 Pin Definitions

3.1 Pin Layout

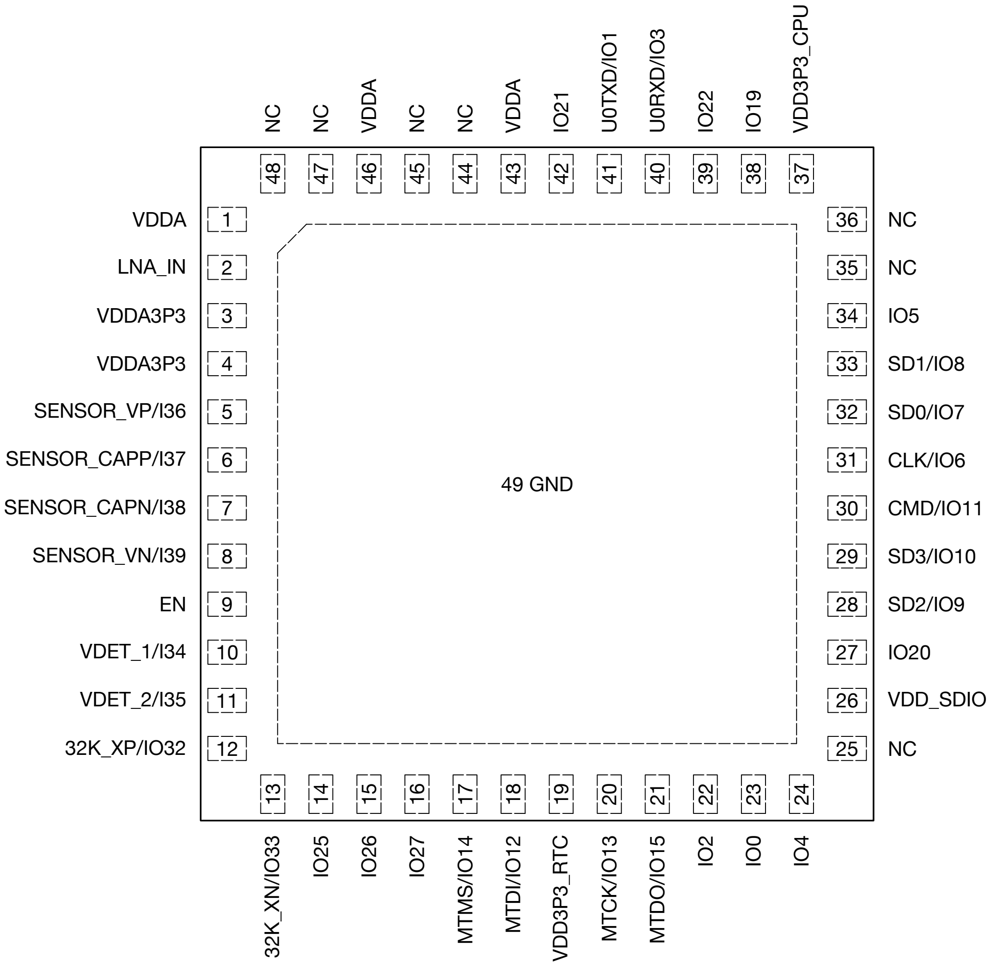


Figure 2: Pin Layout of ESP32-PICO-V3-02 (Top View)

> **Note:**
> The pin diagram shows the approximate location of pins. For the actual mechanical diagram, please refer to Figure 5.

3.2 Pin Description

ESP32-PICO-V3-02 has 48 pins. See pin definitions in Table 1.

Table 1: Pin Definitions

Name	No.	Type	Function
VDDA	1	P	Analog power supply (3.0 V ~ 3.6 V)
LNA_IN	2	I/O	RF input and output
VDDA3P3	3	P	Analog power supply (3.0 V ~ 3.6 V)

Name	No.	Type	Function
VDDA3P3	4	P	Analog power supply (3.0 V ~ 3.6 V)
SENSOR_VP/I36	5	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_CAPP/I37	6	I	GPIO37, ADC1_CH1, RTC_GPIO1
SENSOR_CAPN/I38	7	I	GPIO38, ADC1_CH2, RTC_GPIO2
SENSOR_VN/I39	8	I	GPIO39, ADC1_CH3, RTC_GPIO3
EN	9	I	High: On; enables the SiP Low: Off; the SiP powers off Note: Do not leave this pin floating.
VDET_1/I34	10	I	ADC1_CH6, RTC_GPIO4
VDET_2/I35	11	I	ADC1_CH7, RTC_GPIO5
32K_XP/IO32	12	I/O	32K_XP (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
32K_XN/IO33	13	I/O	32K_XN (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
IO25	14	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	15	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	16	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
MTMS/IO14	17	I/O	ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
MTDI/IO12	18	I/O	ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
VDD3P3_RTC	19	P	Input power supply for RTC IO (3.0 V ~ 3.6 V)
MTCK/IO13	20	I/O	ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
MTDO/IO15	21	I/O	ADC2_CH3, TOUCH3, RTC_GPIO13, MTDO, HSPICS0, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	22	I/O	ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	23	I/O	ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	24	I/O	ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
NC	25	—	NC
VDD_SDIO	26	P	Output power supply. See note 1 under the table.
IO20	27	I/O	GPIO20. See note 3 under the table.
SD2/IO9	28	I/O	See note 2, note 3 under the table.
SD3/IO10	29	I/O	See note 2, note 3 under the table.
CMD/IO11	30	I/O	See note 2, note 3 under the table.
CLK/IO6	31	I/O	See note 2, note 3 under the table.
SD0/IO7	32	I/O	GPIO7, SD_DATA0, HS1_DATA0, U2RTS. See note 3 under the table.
SD1/IO8	33	I/O	GPIO8, SD_DATA1, HS1_DATA1, U2CTS. See note 3 under the table.
IO5	34	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
NC	35	—	NC
NC	36	—	NC
VDD3P3_CPU	37	P	Input power supply for CPU IO (1.8 V ~ 3.6 V)

Name	No.	Type	Function
IO19	38	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
IO22	39	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
U0RXD/IO3	40	I/O	GPIO3, U0RXD, CLK_OUT2
U0TXD/IO1	41	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO21	42	I/O	GPIO21, VSPIHD, EMAC_TX_EN
VDDA	43	P	Analog power supply (3.0 V ~ 3.6 V)
NC	44	—	NC
NC	45	—	NC
VDDA	46	P	Analog power supply (3.0 V ~ 3.6 V)
NC	47	—	NC
NC	48	—	NC

Notice:

1. Note that the embedded flash is connected to VDD_SDIO which is driven directly by VDD3P3_RTC through a 6 Ω resistor. Due to this resistor, there is some voltage drop on this pin from VDD3P3_RTC.
2. Pins CMD/IO11 and CLK/IO6 are used for connecting the embedded flash, and pins SD2/IO9 and SD3/IO10 are used for connecting embeded PSRAM. These pins are not recommended for other uses. For details, please see Section 5 Schematics.
3. IO6/IO7/IO8/IO9/IO10/IO11/IO20 belong to VDD_SDIO power domain and cannot work when VDD_SDIO power shuts down.
4. For peripheral pin configurations, please refer to *ESP32 Datasheet*.

3.3 Compatibility with ESP32-PICO-V3

ESP32-PICO-V3-02 is a new product but it is very similar to ESP32-PICO-V3. It may be possible to update an ESP32-PICO-V3 hardware design to use ESP32-PICO-V3-02 with minimal or no hardware changes, but please pay attention to the following:

- Usage of the following pins has changed:

Table 2: Usage of Pins on ESP32-PICO-V3-02 and ESP32-PICO-V3

Pin No.	ESP32-PICO-V3-02 (embedded flash and PSRAM)	ESP32-PICO-V3 (embedded flash, impossible to connect it with PSRAM)	ESP32-PICO-D4 (embedded flash, possible to connect it with external PSRAM)
25	NC	NC	GPIO16, used to connect embedded flash
27	GPIO20, can be used	GPIO20, can be used	GPIO17, used to connect embedded flash
28	SD2/IO9, used to connect embedded PSRAM, cannot be used externally	SD2/IO9, can be used	GPIO9, can be used

Pin No.	ESP32-PICO-V3-02 (embedded flash and PSRAM)	ESP32-PICO-V3 (embedded flash, impossible to connect it with PSRAM)	ESP32-PICO-D4 (embedded flash, possible to connect it with external PSRAM)
29	SD3/IO10, used to connect embedded PSRAM, cannot be used externally	SD3/IO10, can be used	GPIO10, can be used
32	SD0/IO7, can be used	SD0/IO7, can be used	SD0/IO7, used to connect embedded flash
33	SD1/IO8, can be used	SD1/IO8, can be used	SD1/IO8, used to connect embedded flash
35	NC	NC	GPIO18, can be used
36	NC	NC	GPIO23, can be used

- These three modules vary in size. The size of ESP32-PICO-D4 and ESP32-PICO-V3 is (7 × 7 × 0.94) mm, whereas the size of ESP32-PICO-V3-02 is (7 × 7 × 1.11) mm.
- For security purposes, flash data pins DI, DO, /HOLD, and /WP and PSRAM data pins SI/SIO0, SO/SIO1, SIO2, SIO3 are not led out.
- It is not possible to connect an external PSRAM chip to ESP32-PICO-V3-02 and ESP32-PICO-V3.
- If a 32.768 kHz crystal is connected to ESP32-PICO-D4 then please refer to *ESP32 ECO V3 User Guide* for information about necessary hardware changes for ESP32-PICO-V3-02 and ESP32-PICO-V3.
- Refer to *ESP32 ECO V3 User Guide* for information about possible software changes and optimizations for ESP32 ECO V3.
- EMC compliance and RF performance tests should be repeated after a design is updated to use ESP32-PICO-V3-02.
- Refer to *ESP32-PICO-V3 Datasheet* for more information about ESP32-PICO-V3.
- Refer to *ESP32-PICO-D4 Datasheet* for more information about ESP32-PICO-D4.

3.4 Strapping Pins

ESP32 has five strapping pins: MTDI, GPIO0, GPIO2, MTDO, GPIO5. The pin-pin mapping between ESP32 and the SiP is as follows, which can be seen in Chapter 5 *Schematics*:

- MTDI = IO12
- GPIO0 = IO0
- GPIO2 = IO2
- MTDO = IO15
- GPIO5 = IO5

Software can read the values of these five bits from register ”GPIO_STRAPPING”.

During the chip’s system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of ”0” or ”1”, and hold these bits until the chip is powered down or shut down. The strapping bits configure the device’s boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration by strapping pins.

Table 3: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3 V		1.8 V	
MTDI	Pull-down	0		1	
Booting Mode					
Pin	Default	SPI Boot		Download Boot	
GPIO0	Pull-up	1		0	
GPIO2	Pull-down	Don't-care		0	
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
Pin	Default	U0TXD Active		U0TXD Silent	
MTDO	Pull-up	1		0	
Timing of SDIO Slave					
Pin	Default	FE Sampling FE Output	FE Sampling RE Output	RE Sampling FE Output	RE Sampling RE Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Note:

- FE: falling-edge, RE: rising-edge.
- Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave", after booting.
- The operating voltage of ESP32-PICO-V3-02's integrated external SPI flash and PSRAM is 3.3 V. Therefore, the strapping pin MTDI should hold bit "0" during the SiP power-on reset.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the recommended operating conditions.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	85	°C

Note:
Please see Appendix IO_MUX of *ESP32 Datasheet* for IO's power domain.

4.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T	Operating temperature	–40	—	85	°C
Humidity	Humidity condition	—	50	—	%RH

4.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75×VDD[1]	—	VDD[1]+0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25×VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}	High-level output voltage	0.8×VDD[1]	—	—	V
V_{OL}	Low-level output voltage	—	—	0.1×VDD[1]	V

Symbol	Parameter		Min	Typ	Max	Unit
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain [1,2]	—	40	—	mA
		VDD3P3_RTC power domain [1,2]	—	40	—	mA
		VDD_SDIO power domain [1,3]	—	20	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)		—	28	—	mA
R_{PU}	Resistance of internal pull-up resistor		—	45	—	kΩ
R_{PD}	Resistance of internal pull-down resistor		—	45	—	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to power off the chip		—	—	0.6	V

Note:

1. Please see Appendix IO_MUX of *ESP32 Datasheet* for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, V_{OH}>=2.64 V, as the number of current-source pins increases.
3. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

4.4 Current Consumption Characteristics

With the use of advanced power-management technologies, ESP32 can switch between different power modes.

For details on different power modes, please refer to Section *RTC and Low-Power Management* in *ESP32 Datasheet*.

Table 7: Current Consumption Depending on RF Modes

Work mode	Description		Average (mA)	Peak (mA)
Active (RF working)	TX	802.11b, 20 MHz, 1 Mbps, @19.5 dBm	240	385
		802.11g, 20 MHz, 54 Mbps, @15 dBm	185	270
		802.11b, 20 MHz, MCS7, @13 dBm	180	250
		802.11n, 40 MHz, MCS7, @13 dBm	160	205
	RX	802.11b/g/n, 20 MHz	110	111
		802.11n, 40 MHz	116	117

Note:

- The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 50% duty cycle.
- The current consumption figures for in RX mode are for cases when the peripherals are disabled and the CPU idle.

Table 8: Current Consumption Depending on Work Modes

Work mode	Description		Current consumption (Typ)
Modem-sleep	The CPU is powered on	240 MHz	30 ~ 68 mA
		160 MHz	27 ~ 44 mA
		Normal speed: 80 MHz	20 ~ 31 mA
Light-sleep	—		0.8 mA
Deep-sleep	The ULP co-processor is powered on.		150 μA
	ULP sensor-monitored pattern		100 μA @1% duty
	RTC timer + RTC memory		10 μA
	RTC timer only		5 μA
Power off	CHIP_PU is set to low level, the chip is powered off.		1 μA

Note:

- The current consumption figures in Modem-sleep mode are for cases where the CPU is powered on and the cache idle.
- When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, current consumption changes accordingly.
- In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.
- During Deep-sleep, when the ULP co-processor is powered on, peripherals such as GPIO and I²C are able to operate.
- The "ULP sensor-monitored pattern" refers to the mode where the ULP coprocessor or the sensor works periodically. When ADC works with a duty cycle of 1%, the typical current consumption is 100 μA.

4.5 Wi-Fi RF Characteristics

4.5.1 Wi-Fi RF Standards

Table 9: Wi-Fi RF Standards

Name		Description
Center frequency range of operating channel ^{note1}		2412 ~ 2484 MHz
Wi-Fi wireless standard		IEEE 802.11b/g/n
Data rate	20 MHz	11b: 1, 2, 5.5 and 11 Mbps 11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 11n: MCS0-7, 72.2 Mbps (Max)
	40 MHz	11n: MCS0-7, 150 Mbps (Max)

Note:

1. Device should operate in the center frequency range allocated by regional regulatory authorities. Target center frequency range is configurable by software.
2. For the SiPs that use IPEX antennas, the output impedance is 50 Ω. For other SiPs without IPEX antennas, users do not need to concern about the output impedance.

4.5.2 Transmitter Characteristics

Table 10: Transmitter Characteristics

Parameter	Rate	Typ	Unit
TX Power ^{note}	11b, 1 Mbps	19.5	dBm
	11b, 11 Mbps	19.5	
	11g, 6 Mbps	18	
	11g, 54 Mbps	14	
	11n, HT20, MCS0	18	
	11n, HT20, MCS7	13	
	11n, HT40, MCS0	18	
	11n, HT40, MCS7	13	

Note:
Target TX power is configurable based on device or certification requirements.

4.5.3 Receiver Characteristics

Table 11: Receiver Characteristics

Parameter	Rate	Typ	Unit
RX Sensitivity	1 Mbps	–97	dBm
	2 Mbps	–94	
	5.5 Mbps	–92	
	11 Mbps	–88	
	6 Mbps	–93	
	9 Mbps	–91	
	12 Mbps	–89	
	18 Mbps	–87	
	24 Mbps	–84	
	36 Mbps	–80	
	48 Mbps	–77	
	54 Mbps	–75	
	11n, HT20, MCS0	–92	
	11n, HT20, MCS1	–88	
	11n, HT20, MCS2	–86	
	11n, HT20, MCS3	–83	
	11n, HT20, MCS4	–80	
	11n, HT20, MCS5	–76	
	11n, HT20, MCS6	–74	
	11n, HT20, MCS7	–72	
	11n, HT40, MCS0	–89	
	11n, HT40, MCS1	–85	
	11n, HT40, MCS2	–83	
	11n, HT40, MCS3	–80	

Parameter	Rate	Typ	Unit
	11n, HT40, MCS4	–76	
	11n, HT40, MCS5	–72	
	11n, HT40, MCS6	–71	
	11n, HT40, MCS7	–69	
RX Maximum Input Level	11b, 1 Mbps	5	dBm
	11b, 11 Mbps	5	
	11g, 6 Mbps	0	
	11g, 54 Mbps	–8	
	11n, HT20, MCS0	0	
	11n, HT20, MCS7	–8	
	11n, HT40, MCS0	0	
	11n, HT40, MCS7	–8	
Adjacent Channel Rejection	11b, 11 Mbps	35	dB
	11g, 6 Mbps	27	
	11g, 54 Mbps	13	
	11n, HT20, MCS0	27	
	11n, HT20, MCS7	12	
	11n, HT40, MCS0	16	
	11n, HT40, MCS7	7	

4.6 Bluetooth Radio

4.6.1 Receiver – Basic Data Rate

Table 12: Receiver Characteristics – Basic Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @0.1% BER	—	–90	–89	–88	dBm
Maximum received signal @0.1% BER	—	0	—	—	dBm
Co-channel C/I	—	—	+7	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	—	–6	dB
	F = F0 – 1 MHz	—	—	–6	dB
	F = F0 + 2 MHz	—	—	–25	dB
	F = F0 – 2 MHz	—	—	–33	dB
	F = F0 + 3 MHz	—	—	–25	dB
	F = F0 – 3 MHz	—	—	–45	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	—	—	dBm
	2000 MHz ~ 2400 MHz	–27	—	—	dBm
	2500 MHz ~ 3000 MHz	–27	—	—	dBm
	3000 MHz ~ 12.5 GHz	–10	—	—	dBm
Intermodulation	—	–36	—	—	dBm

4.6.2 Transmitter – Basic Data Rate

Table 13: Transmitter Characteristics – Basic Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power (see note under Table 13)	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
+20 dB bandwidth	—	—	0.9	—	MHz
Adjacent channel transmit power	F = F0 ± 2 MHz	—	–55	—	dBm
	F = F0 ± 3 MHz	—	–55	—	dBm
	F = F0 ± > 3 MHz	—	–59	—	dBm
$\Delta\ f1_{\text{avg}}$	—	—	—	155	kHz
$\Delta\ f2_{\text{max}}$	—	127	—	—	kHz
$\Delta\ f2_{\text{avg}}/\Delta\ f1_{\text{avg}}$	—	—	0.92	—	—
ICFT	—	—	–7	—	kHz
Drift rate	—	—	0.7	—	kHz/50 μs
Drift (DH1)	—	—	6	—	kHz
Drift (DH5)	—	—	6	—	kHz

Note:
There are a total of eight power levels from 0 to 7, and the transmit power ranges from –12 dBm to 9 dBm. When the power level rises by 1, the transmit power increases by 3 dB. Power level 4 is used by default and the corresponding transmit power is 0 dBm.

4.6.3 Receiver – Enhanced Data Rate

Table 14: Receiver Characteristics – Enhanced Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
$\pi/4$ DQPSK					
Sensitivity @0.01% BER	—	–90	–89	–88	dBm
Maximum received signal @0.01% BER	—	—	0	—	dBm
Co-channel C/I	—	—	11	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–7	—	dB
	F = F0 – 1 MHz	—	–7	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–35	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–45	—	dB
8DPSK					
Sensitivity @0.01% BER	—	–84	–83	–82	dBm
Maximum received signal @0.01% BER	—	—	–5	—	dBm
C/I c-channel	—	—	18	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	2	—	dB
	F = F0 – 1 MHz	—	2	—	dB
	F = F0 + 2 MHz	—	–25	—	dB

Parameter	Conditions	Min	Typ	Max	Unit
	F = F0 – 2 MHz	—	–25	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–38	—	dB

4.6.4 Transmitter – Enhanced Data Rate

Table 15: Transmitter Characteristics – Enhanced Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power (see note under Table 13)	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
$\pi/4$ DQPSK max w0	—	—	–0.72	—	kHz
$\pi/4$ DQPSK max wi	—	—	–6	—	kHz
$\pi/4$ DQPSK max |wi + w0|	—	—	–7.42	—	kHz
8DPSK max w0	—	—	0.7	—	kHz
8DPSK max wi	—	—	–9.6	—	kHz
8DPSK max |wi + w0|	—	—	–10	—	kHz
$\pi/4$ DQPSK modulation accuracy	RMS DEVM	—	4.28	—	%
	99% DEVM	—	100	—	%
	Peak DEVM	—	13.3	—	%
8 DPSK modulation accuracy	RMS DEVM	—	5.8	—	%
	99% DEVM	—	100	—	%
	Peak DEVM	—	14	—	%
In-band spurious emissions	F = F0 ± 1 MHz	—	–46	—	dBm
	F = F0 ± 2 MHz	—	–44	—	dBm
	F = F0 ± 3 MHz	—	–49	—	dBm
	F = F0 +/– > 3 MHz	—	—	–53	dBm
EDR differential phase coding	—	—	100	—	%

4.7 Bluetooth LE Radio

4.7.1 Receiver

Table 16: Receiver Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	–94	–93	–92	dBm
Maximum received signal @30.8% PER	—	0	—	—	dBm
Co-channel C/I	—	—	+10	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–5	—	dB
	F = F0 – 1 MHz	—	–5	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–35	—	dB

Parameter	Conditions	Min	Typ	Max	Unit
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–45	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	—	—	dBm
	2000 MHz ~ 2400 MHz	–27	—	—	dBm
	2500 MHz ~ 3000 MHz	–27	—	—	dBm
	3000 MHz ~ 12.5 GHz	–10	—	—	dBm
Intermodulation	—	–36	—	—	dBm

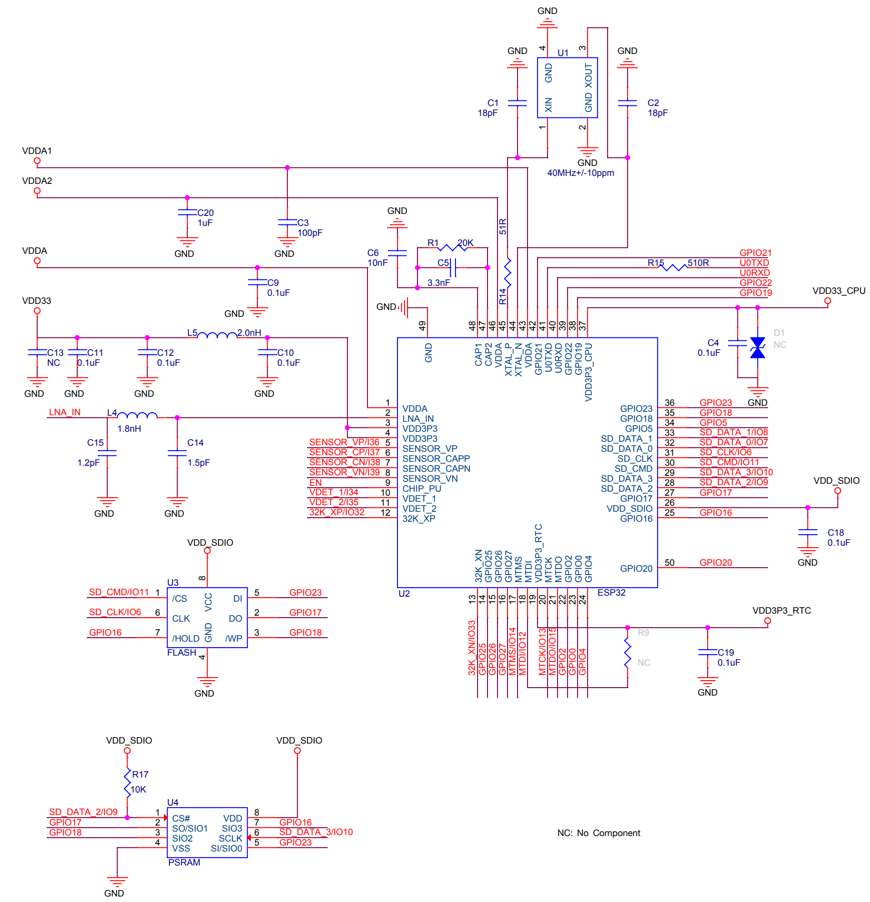
4.7.2 Transmitter

Table 17: Transmitter Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power (see note under Table 13)	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
Adjacent channel transmit power	F = F0 ± 2 MHz	—	–55	—	dBm
	F = F0 ± 3 MHz	—	–57	—	dBm
	F = F0 ± > 3 MHz	—	–59	—	dBm
$\Delta f1_{avg}$	—	—	—	265	kHz
$\Delta f2_{max}$	—	210	—	—	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	—	—	+0.92	—	—
ICFT	—	—	–10	—	kHz
Drift rate	—	—	0.7	—	kHz/50 μs
Drift	—	—	2	—	kHz

5 Schematics

This is the reference design of the SiP.



Pin Mapping

ESP32	ESP32-PICO-V3-02
VDDA	VDDA
LNA_IN	LNA_IN
VDD3P3	VDD3P3
VDD3P3	VDD3P3
SENSOR_VP	SENSOR_VP
SENSOR_CAPP	SENSOR_CAPP
SENSOR_CAPN	SENSOR_CAPN
SENSOR_VN	SENSOR_VN
CHIP_PU	EN
VDET_1	VDET_1
VDET_2	VDET_2
32K_XP	32K_XP
32K_XN	32K_XN
GPIO25	IO25
GPIO26	IO26
GPIO27	IO27
MTMS	MTMS
MTDI	MTDI
VDD3P3_RTC	VDD3P3_RTC
MTCK	MTCK
MTDO	MTDO
GPIO2	IO2
GPIO0	IO0
GPIO4	IO4
GPIO16	NC
VDD_SDIO	VDD_SDIO
GPIO17	NC
SD_DATA_2	SD_DATA_2
SD_DATA_3	SD_DATA_3
SD_CMD	SD_CMD
SD_CLK	SD_CLK
SD_DATA_0	SD_DATA_0
SD_DATA_1	SD_DATA_1
GPIO5	IO5
GPIO18	NC
GPIO23	NC
VDD3P3_CPU	VDD3P3_CPU
GPIO19	IO19
GPIO22	IO22
U0RXD	U0RXD
U0TXD	U0TXD
GPIO21	IO21
VDDA	VDDA
XTAL_N	NC
XTAL_P	NC
VDDA	VDDA
CAP2	NC
CAP1	NC
GND	GND
	IO20

Figure 3: ESP32-PICO-V3-02 Schematics

6 Peripheral Schematics

This is the typical application circuit of the SiP connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

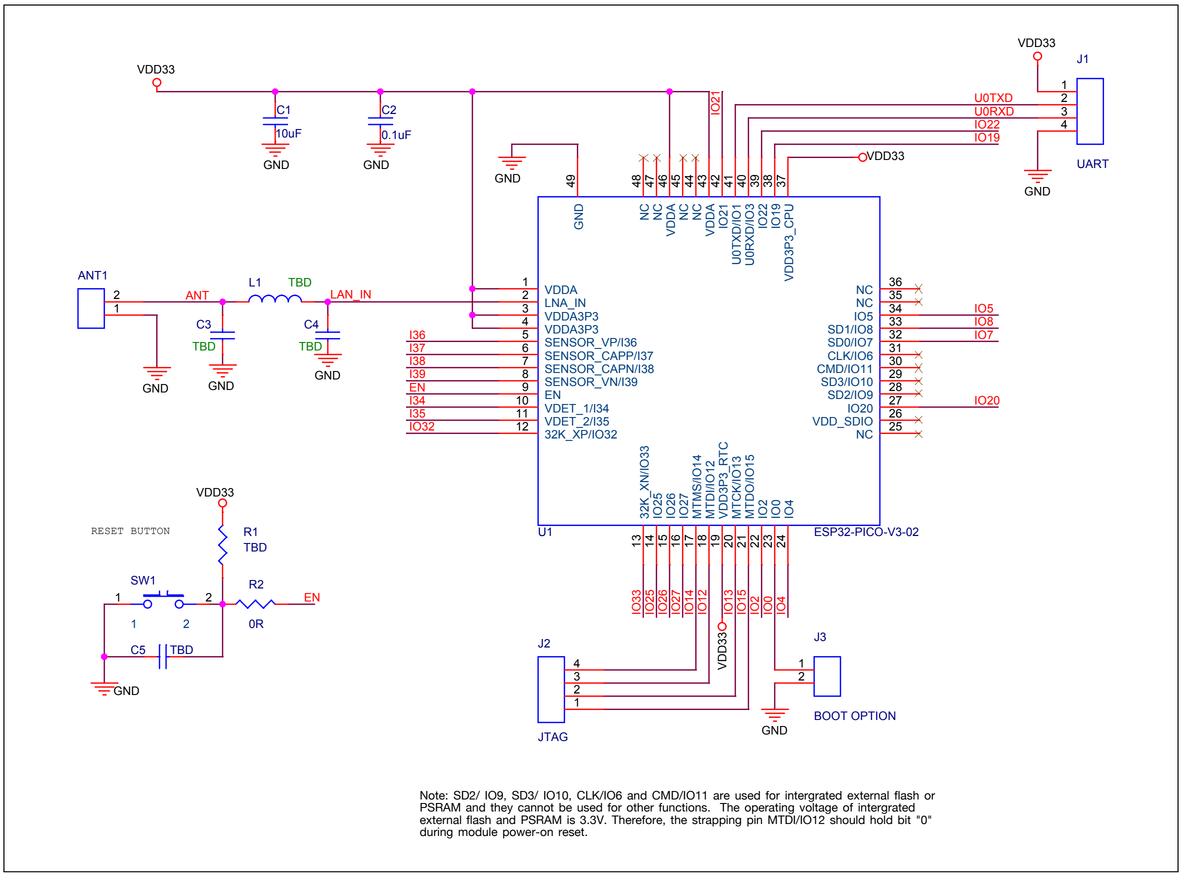


Figure 4: ESP32-PICO-V3-02 Peripheral Schematics

> **Note:**
> To ensure the power supply to the ESP32 chip during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the SiP and the power-up and reset sequence timing of the chip. For ESP32's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in *ESP32 Datasheet*.

7 Package Information

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.010	1.110	1.210	0.040	0.044	0.048
c	0.220	0.260	0.300	0.009	0.010	0.012
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	4.850	4.950	5.050	0.191	0.195	0.199
E1	4.850	4.950	5.050	0.191	0.195	0.199
H	---	0.300	---	---	0.012	---
H1	---	0.300	---	---	0.012	---
L	0.325	0.400	0.475	0.013	0.016	0.019
L1	0.000	0.075	0.150	0.000	0.003	0.006
L2	0.950	1.025	1.100	0.037	0.040	0.043
L3	0.950	1.025	1.100	0.037	0.040	0.043
e	---	0.500	---	---	0.020	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.150			0.006		

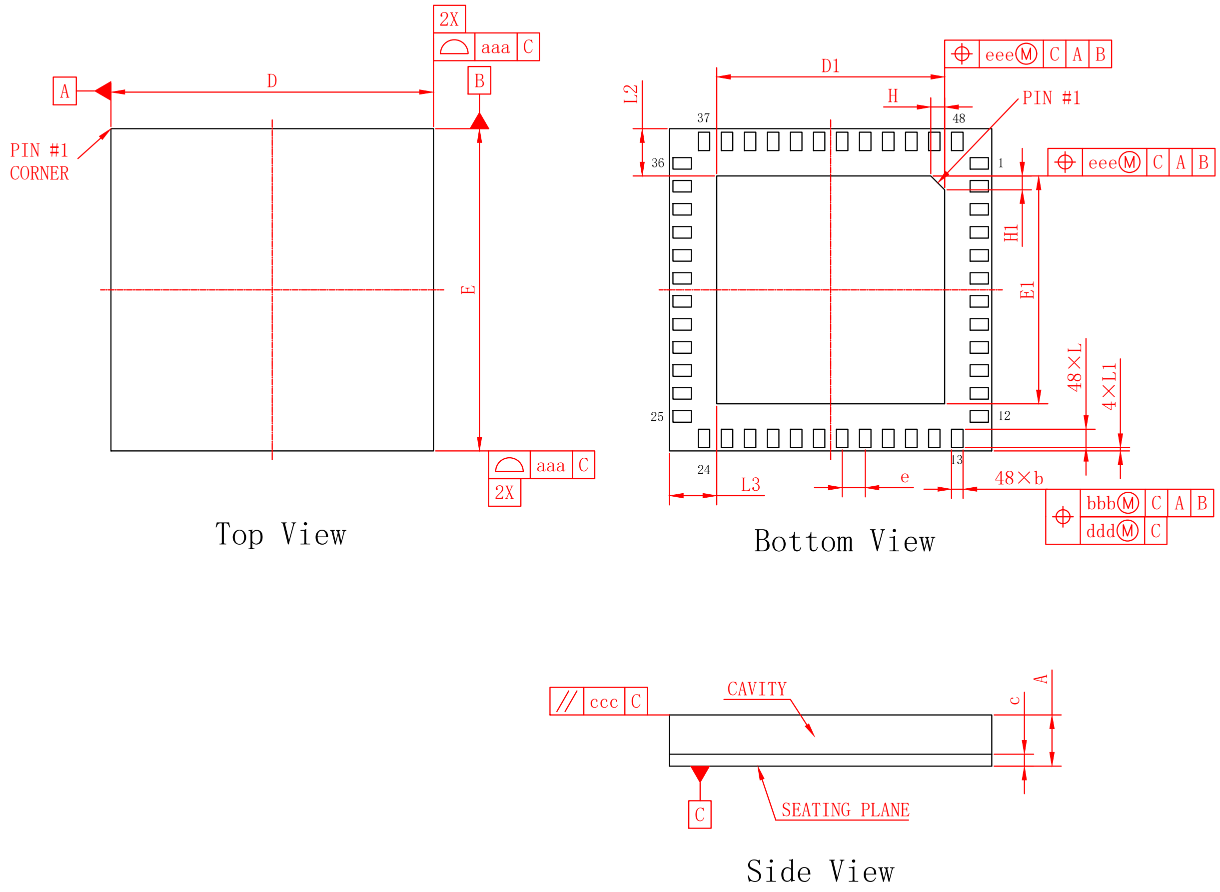
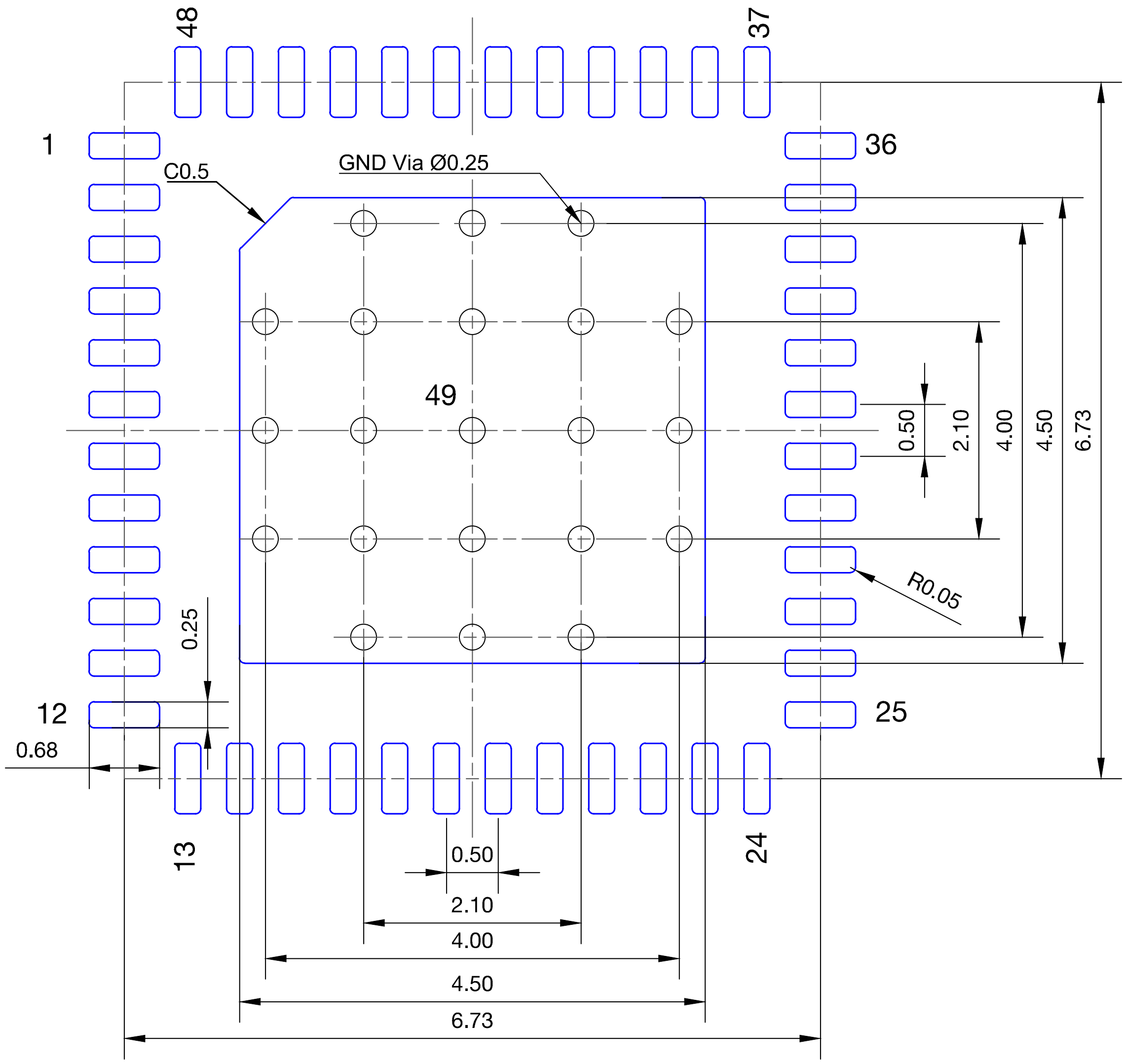
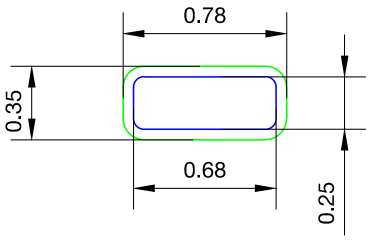
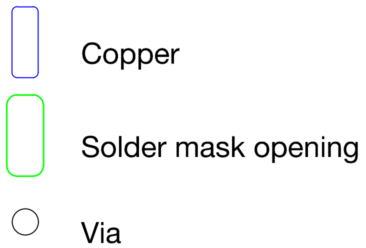


Figure 5: ESP32-PICO-V3-02 Package





Details of recommended copper-defined pad.

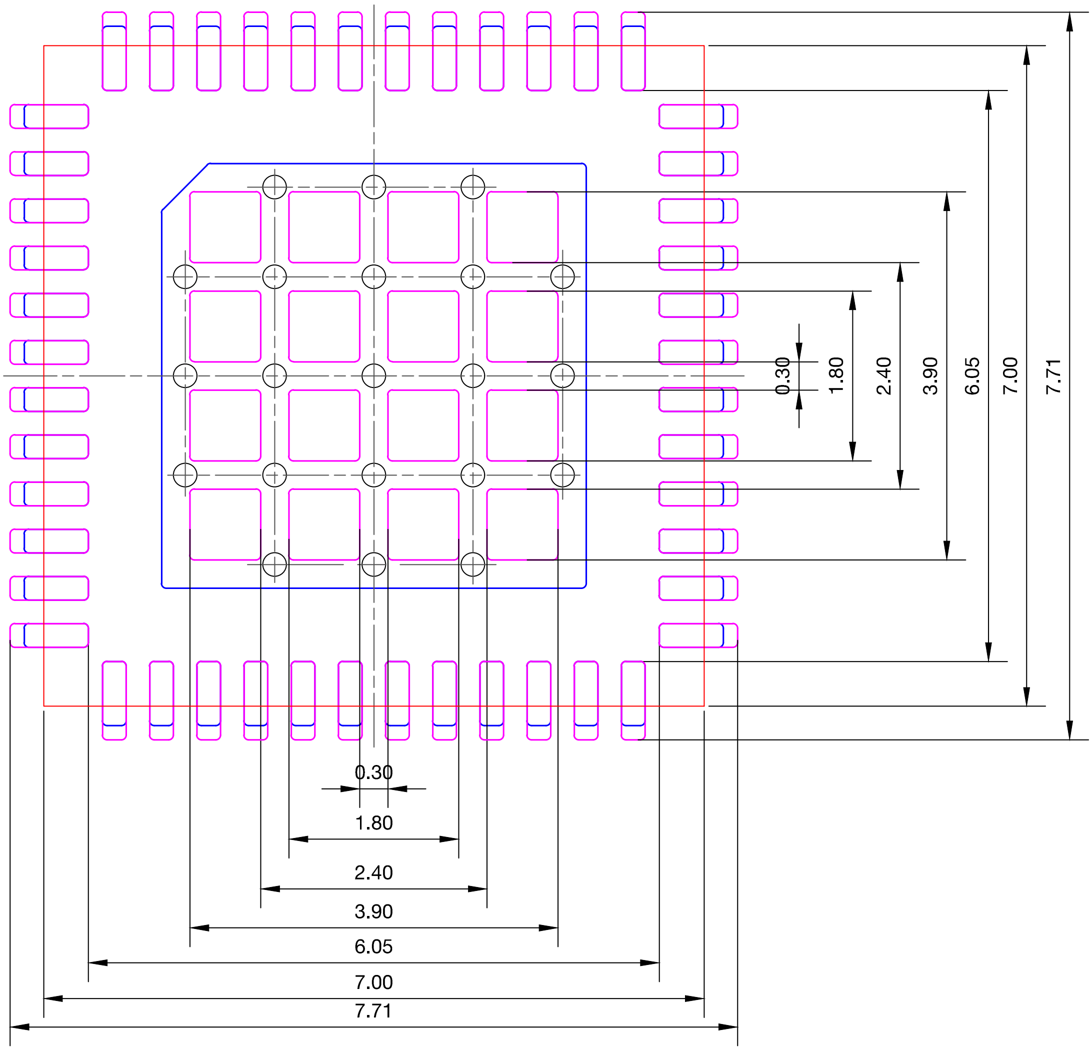


Unit: mm
Tolerance: +/- 0.05 mm

Notes:

1. It is recommended to use copper-defined pad for Pin 1 to Pin 48 and solder-mask-defined pad for Pin 49 (thermal pad).
2. This drawing is subject to change without notice.

Figure 6: ESP32-PICO-V3-02 PCB Land Pattern



Notes:

1. It is recommended to use a stencil of 80 um thickness.
2. This drawing is subject to change without notice.

Copper

Paste mask opening

Recommended via drill size: 0.25 mm

Unit: mm

Tolerance: +/- 0.05 mm

Figure 7: ESP32-PICO-V3-02 STENCIL

8 Product Handling

8.1 Storage Condition

The products sealed in Moisture Barrier Bag (MBB) should be stored in a noncondensing atmospheric environment of < 40 °C/90%RH.

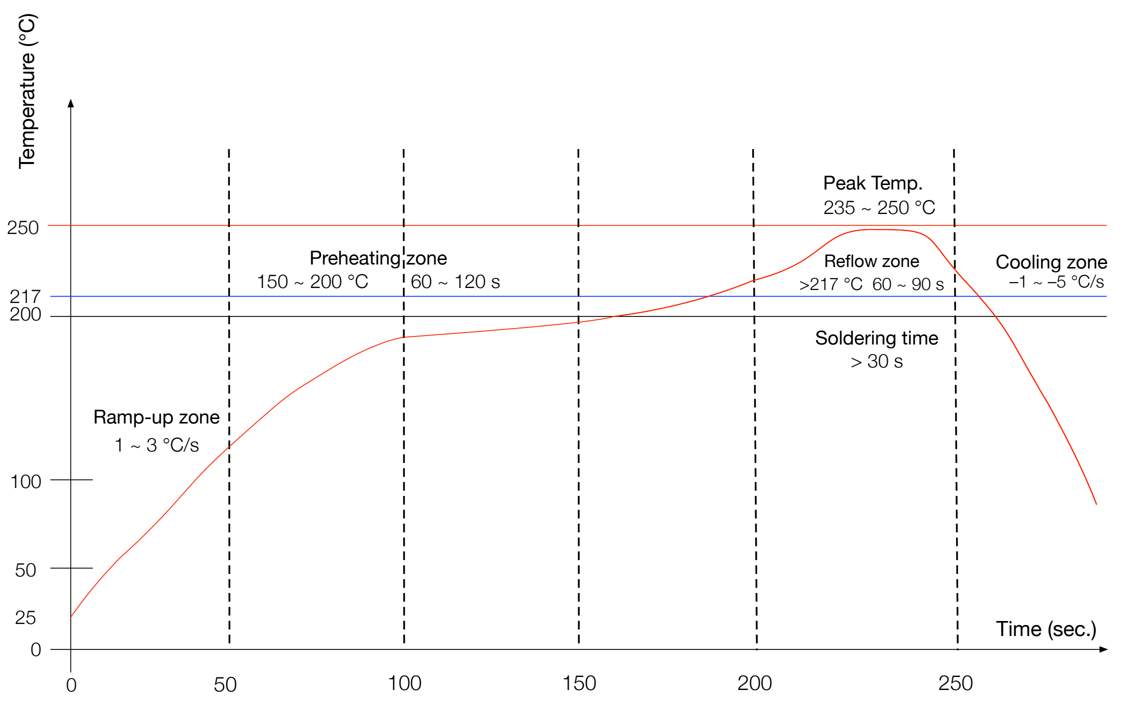
The SiP is rated at moisture sensitivity level (MSL) 3.

After unpacking, the SiP must be soldered within 168 hours with factory conditions 25±5 °C and 60% RH. The SiP needs to be baked if the above conditions are not met.

8.2 ESD

- Human body model (HBM): 2000 V
- Charged-device model (CDM): 500 V

8.3 Reflow Profile



Ramp-up zone — Temp.: 25 ~ 150 °C Time: 60 ~ 90 s Ramp-up rate: 1 ~ 3 °C/s
Preheating zone — Temp.: 150 ~ 200 °C Time: 60 ~ 120 s
Reflow zone — Temp.: >217 °C Time: 60 ~ 90 s; Peak Temp.: 235 ~ 250 °C Time: 30 ~ 70 s
Cooling zone — Peak Temp. ~ 180 °C Ramp-down rate: −1 ~ −5 °C/s
Solder — Sn-Ag-Cu (SAC305) lead-free solder alloy

Figure 8: Reflow Profile

> **Note:**
> Solder the SiP in a single reflow.

9 MAC Addresses and eFuse

The eFuse in ESP32 has been burnt into 48-bit mac_address. The actual addresses the chip uses in station, AP, BLE, and Ethernet modes correspond to mac_address in the following way:

- Station mode: mac_address
- AP mode: mac_address + 1
- BLE mode: mac_address + 2
- Ethernet mode: mac_address + 3

In the 1 Kbit eFuse, 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash-encryption and chip-ID.

10 Learning Resources

10.1 Must-Read Documents

The following link provides documents related to ESP32.

- *ESP32 Datasheet*
  This document provides an introduction to the specifications of the ESP32 hardware, including overview, pin definitions, functional description, peripheral interface, electrical characteristics, etc.
- *ESP32 ECO V3 User Guide*
  This document describes differences between V3 and previous ESP32 silicon wafer revisions.
- *ECO and Workarounds for Bugs in ESP32*
  This document details hardware errata and workarounds in the ESP32.
- *ESP-IDF Programming Guide*
  It hosts extensive documentation for ESP-IDF ranging from hardware guides to API reference.
- *ESP32 Technical Reference Manual*
  The manual provides detailed information on how to use the ESP32 memory and peripherals.
- ESP32 Hardware Resources
  The zip files include the schematics, PCB layout, Gerber and BOM list of ESP32 modules and development boards.
- *ESP32 Hardware Design Guidelines*
  The guidelines outline recommended design practices when developing standalone or add-on systems based on the ESP32 series of products, including the ESP32 chip, the ESP32 modules and development boards.
- *ESP32 AT Instruction Set and Examples*
  This document introduces the ESP32 AT commands, explains how to use them, and provides examples of several common AT commands.
- *Espressif Products Ordering Information*

10.2 Must-Have Resources

Here are the ESP32-related must-have resources.

- ESP32 BBS
  This is an Engineer-to-Engineer (E2E) Community for ESP32 where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
- ESP32 GitHub
  ESP32 development projects are freely distributed under Espressif's MIT license on GitHub. It is established to help developers get started with ESP32 and foster innovation and the growth of general knowledge about the hardware and software surrounding ESP32 devices.
- ESP32 Tools
  This is a webpage where users can download ESP32 Flash Download Tools and the zip file "ESP32 Certification and Test".

- ESP-IDF
  This webpage links users to the official IoT development framework for ESP32.
- ESP32 Resources
  This webpage provides the links to all available ESP32 documents, SDK and tools.

Revision History

Date	Version	Release notes
2021-02-09	V0.6	Added Figure 6 and Figure 7. Deleted Reset Circuit and Discharge Circuit for VDD33 Rail. Updated the C value in RC delay circuit from 0.1 μF to 1 μF. Modified the note below Figure 8: *Reflow Profile*. Added TWAI® in Section 1.1: *Features*.
2020-08-04	V0.5	Preliminary release.